SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

# THERMAL MANAGEMENT IN SURFACE MOUNTING

The evolutionary trends of integrated circuits and printed circuits boards are, in both cases, towards improved performance and reduced size. From these points of view, a factor of major importance has been mutual thermal interaction between ICs, even those with low dissipation.

It follows then that thermal design of medium and high density applications has evolved to include factors such as power effects, die size, package thermal resistance, **integration level of active devices** and substrate type. Added to this a trend towards greater use of switching techniques exists.

Today, in order to design reliable application circuits, it is necessary to have complete data on package thermal response characteristics. In fact, it is a well known and long established fact that device lifetime has an exponential relationship with junction temperature.

## PRELIMINARY CONSIDERATIONS

Heat dissipation for DIPs with a low thermal conductivity frame (e.g. Alloy42) is due to convection and **irradiation** from an emiting area corresponding to the silicon die and the package die pad.

Since heat transmission through the lead frame is very poor, dissipation does not depend greatly on substrate type. In fact, samples soldered on printed circuit boards, or inserted in **connectors** have nearly the same dissipation capability as samples suspended in air. The difference, in the range of just 10%, is commonly ignored and specifications for insertion ICs only give one thermal resistance value, which is more than adequate for good thermal design.

The question then arises, is the approximation valid for SO and PLCC packages ?

The answer is no ! Thermal characteristics for these devices are influenced by many factors.

1) Device Related Factors
   - size of the dissipating element
   - dissipation level
   - pulse length and duty cycle

2) Package Related Factors
   - thermal conductivity of the frame
   - frame design

3) Substrate Related Factors
   - thermal conductivity of the substrate
   - layout

Therefore a number of parameters can change the thermal characteristics. These cannot be described by a single thermal resistance, in fact a set of experimental curves gives the best presentation.

## JUNCTION TO AMBIENT THERMAL RESISTANCE $R_{th(j-a)}$

$R_{th(j-a)}$ represents the thermal resistance of the system and comprises the silicon die, the package, and any thermal mass in contact with the package to dissipate heat to the ambient.

At a given dissipation level $P_d$, the increase in junction temperature $\Delta T_j$ over ambient temperature $T_a$ is given by :

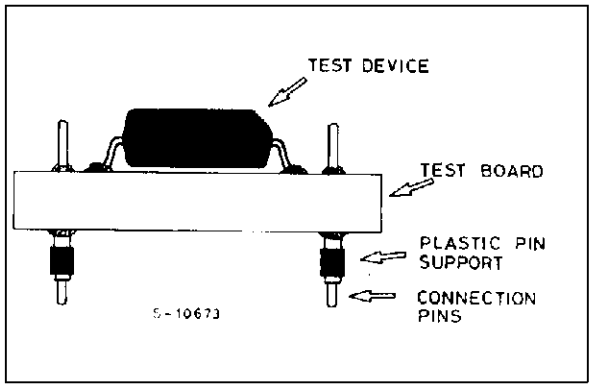
$\Delta T_j = R_{th(j-a)} \times P_d$

$R_{th(j-a)}$ is made up of many elements both within the device and external to it.

If the device is considered alone, $R_{th(j-a)}$ is given by the dissipation path from the silicon die to the leadframe, to the molding compound, to the ambient. **Experimental values are very large in this condition, especially for small packages such as Small Outline types.**

However, this situation is not met in practice and experimental data included in the present work indicates the worst case (floating samples). In most applications, Surface Mount Devices are soldered onto a substrate (commonly epoxy glass (FR4) and are in thermal contact with it through the soldered joints and the copper interconnections. In this case, the heat generated by the active circuit is transferred to the leadframe and then to the substrate. A new dissipation path thus exists in parallel with the previous one whose efficiency depends on the thermal conductivity of the frame and on the length of the printed circuit's copper tracks. Figure A shows the experimental module.

**Figure A :** Device Soldered to the Best Board, for Junction to Ambient Thermal Resistance Measurement.

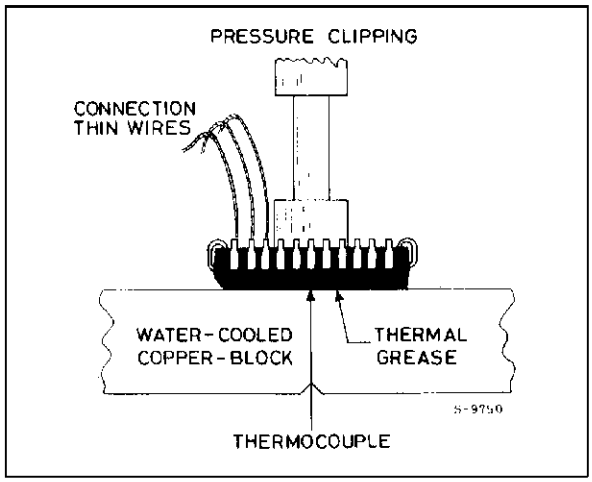



## JUNCTION TO CASE THERMAL RESISTANCE $R_{th(j-c)}$

$R_{th(j-c)}$ is the thermal resistance from the junction to a given area of the peackage's external surface where a heatsink is applied.

In signal packages, a suitable area is its upper surface. **Measurements are made with the samples in good thermal contact with an infinite heatsink (fig. B).**

**Figure B :** Junction to Case Thermal Resistance Measurement.




When a heatsink of thermal resistance $R_{hs}$ is attached to the package, the following relationship is valid :

$$R_{th(j-a)} = R_{th(j-c)} + \frac{R_{hs} \times R^*}{R_{hs} + R^*}$$

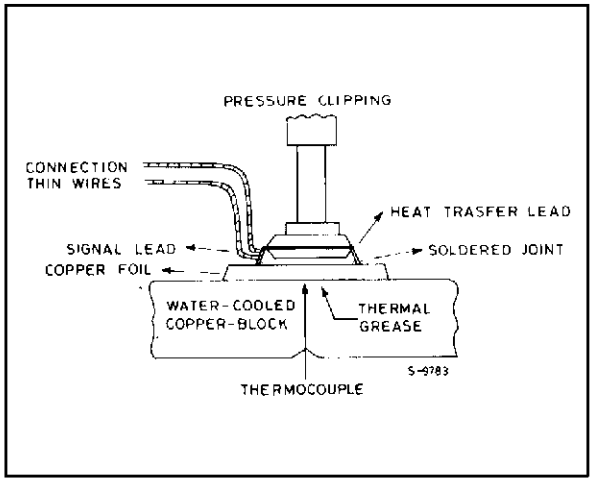
Where $R^*$ takes into account all the other dissipation paths (i.e. junction/frame/substrate). $R^*$ is the lowest with low thermal conductivity frames.

In high power applications $R^*$ " $R_{hs}$ and $R_{th(j-a)} = R_{th(j-c)} + R_{hs}$

## JUNCTION TO PIN THERMAL RESISTANCE $R_{th(j-p)}$

In medium power packages $R_{th(j-p)}$ is the thermal resistance of the heat transfer leads, from the junction to the external heatsink. In most cases the external heatsink is integrated on the board. Figure C shows the experimental setup.

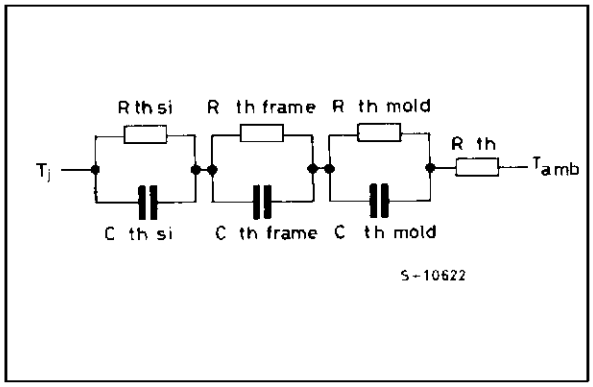
**Figure C :** Junction to Pin Thermal Resistance Measurement.




## TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

The electrical equivalent of heat dissipation for a module formed by an active device, its package, a PCB and the ambient, is a chain of RC cells, as shown in fig. D, each with a characteristic rise time ($\tau$) = RC.

**Figure D :** Equivalent Thermal Circuit Simplified Package.

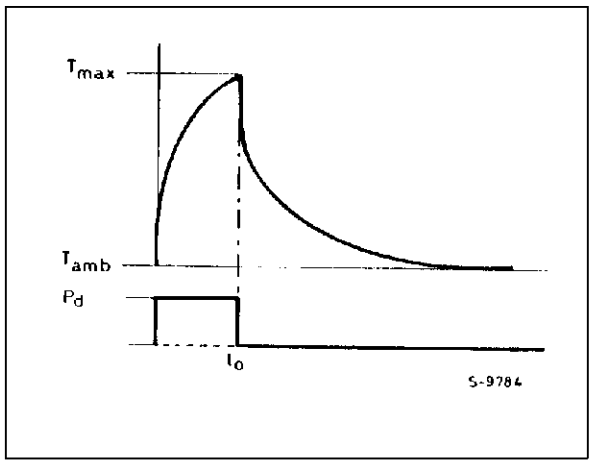


The thermal capacitance of each cell is a measure of its ability to accumulate heat and depends on the specific heat, volume and density of the constituent materials.

When power is switched on, the junction temperature after time it is governed by the heat impedance of the cells, each of which follows its own time constant - this is analogous to the exponential charge of RC cells in an electrical circuit.

For a pulse lenght $t_o$, the effective $T_j$ can be significantly lower than the steady state $T_j$ (fig. E) and the transient thermal resistance $R_{th(to)}$ can be defined from the ratio between the junction temperature at the end of the pulse and the dissipated power.

**Figure E :** Temperature Rise for Single Power Pulse.




Obviously, this parameter is smaller for shorter pulses and higher power can be dissipated without exceeding the maximum junction temperature defined from a reliability point of view.

The knowledge of transient thermal data is an important tool for cost effective thermal design of switching applications.

## PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

When pulses of the same height Pd are repeated with a duty cycle, DC, and a pulse width $t_o$, which is shorter than the overall system time constant, the train of pulses is seen as a continuous source of mean power $Pd_{avg}$, where :

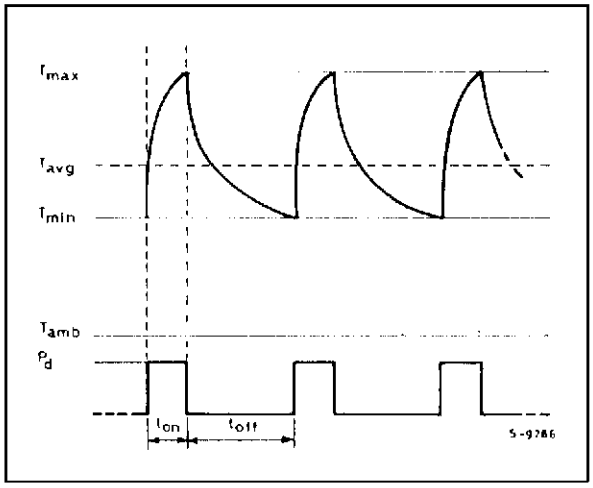
$Pd_{avg} = Pd \times DC$

However the silicon die has a time constant in the order of 1 to 2ms and is able to follow frequencies in the kHz range. Thus junction temperature oscillates about an average value given by :

$T_{javg} = R_{th} \times Pd_{avg}$

as is graphically shown in fig. F.

**Figure F :** Temperature Rise for Repeated Power Pulses.




The thermal resistance corresponding to the peak of the steady state oscillations (peak thermal resis-tance indicates the maximum temperature reached by the junction and, depending on duty cycle and pulse width, may be much lower than the DC thermal resistance.

## EXPERIMENTAL METHOD

Measurements were performed by means of the especially developed thermal test pattern P432, which is designed according to the Semiconductor Equipment and Materials Institute (SEMI) G32 guideline.

Test chip P432 is based on a dissipating element formed by two npn transistors, each with 10W power capability, and one sensing diode (fig. G). The diode is placed on the temperature plateau generated when the two transistors are biased in parallel, and gives the actual junction temperature $T_j$ of the dissipating element, through the calibration curve (fig. H) of its forward voltage Vf versus temperature at a constant current of 100µA.

**Figure G :** Thermal Test Pattern P432.

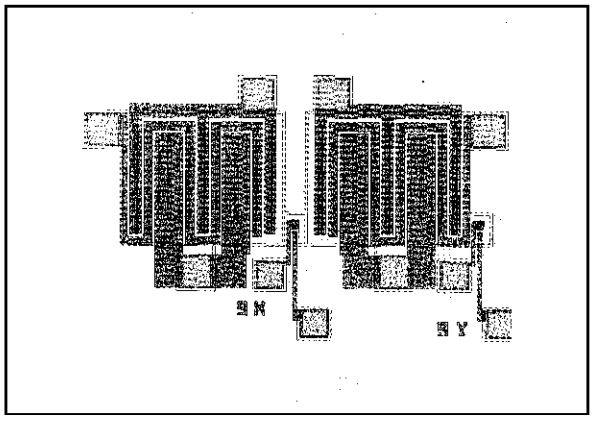
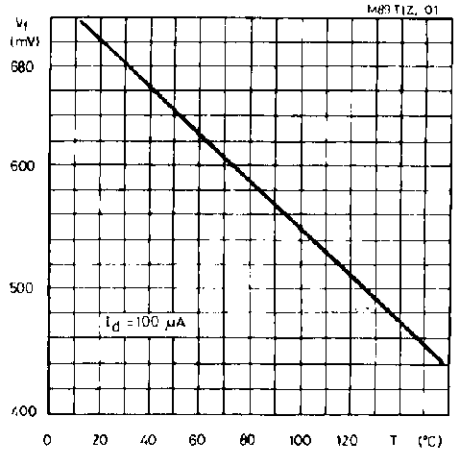


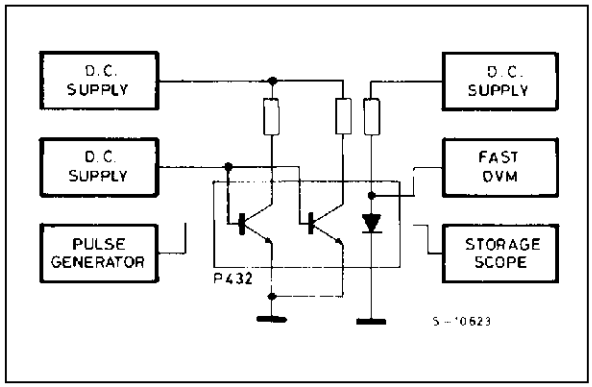
**Figure H :** Calibration Curve of P432 Temperature Sensing Diode.




Transistor size is intentionally limited to 1000sq. mils, in order to simulate high power density, characterizing a worst case. Die size, which is found to have little influence on thermal resistance when a copper frame is used, is slightly smaller than the die pad size and never exceeds 30k sq mils even in the largest packages such as high pin count PLCCs.

The measurement setup is shown in fig. I. it is compatible with DC and AC supplies and has an accuracy of better than 5%.

**Figure I :** Experimental Setup.




The advantages offered by the test pattern are :

- high power capability
- repeatable $V_f$ and temperature coefficient (1.9mv/C) of the sensing element
- high resolution in pulsed conditions (100µs)
- better correlation from one package to another.

Both Alloy 42 and copper frames were considered for narrow SO packages (150mils body). For wide SO (300mils body) and PLCC packages only copper frames were examined. Suitable test boards were developed (figs J, K and L).

**Figure J :** Test Board Lay-out for SO Packages (150 mils body width) Board size is : 23 x 42mm$^2$.

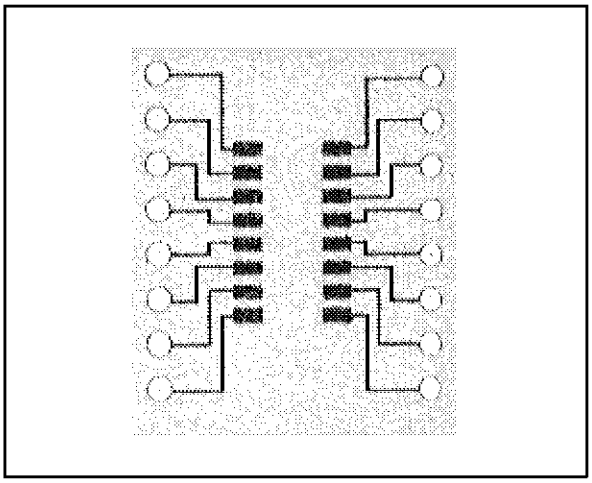


**Figure K :** Test Board Lay-out for SO Packages (3000 mils body width) Board size is 38 x 43mm$^2$.

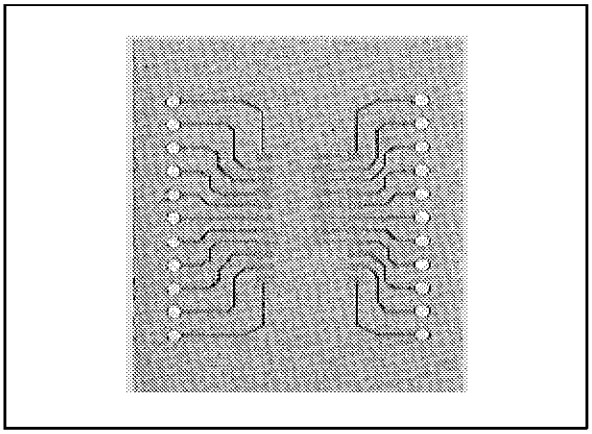
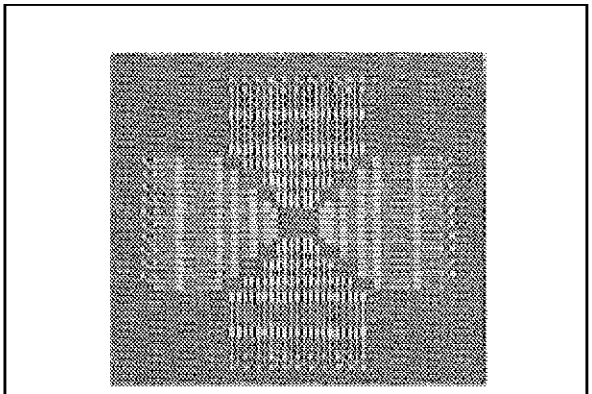


**Figure K :** Test Board for PLCCs Board size is 58 x 58mm$^2$.



## MEDIUM POWER PACKAGES

While surface mount signal ICs are readily available, almost all power ICs are still assembled in traditional insertion packages.

Medium power SM packages (Pd < 2W) can readily be derived from existing small outline and chip carrier packages by modifying the leadframe - in much the same way that Powerdip packages were derived from standard Dips.

This approach is particularly attractive because the external dimensions of the package are identical to existing low power packages, allowing the use of standard automatic assembly and test equipment. Frame modification is aimed at obtaining a low junction to pin thermal resistance path for the transfer of heat to a suitable external heatsink. A number of leads are connected to the die pad for this purpose. Two possibilities are considered here : a medium power PLCC44 with 11 heat transfer leads (fig. M) and a medium power SO20 with 8 heat transfer leads (fig. N).

A cost effective heat spreader can be obtained on the board by means of suitably dimensioned copper areas. The heat transfer leads are soldered to there areas (fig. M1, N1).

**Figure M :** Lead Frame for Medium Power PLCC44.

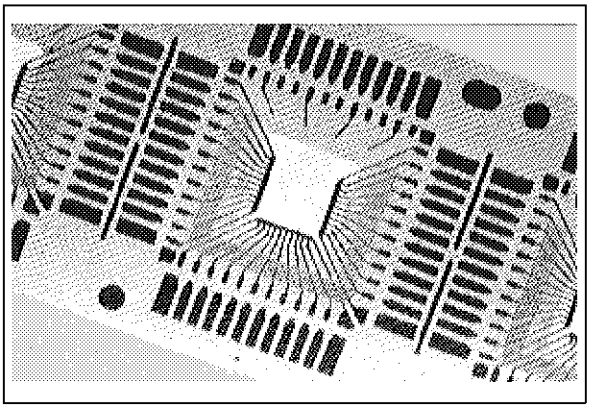


**Figure N :** Lead Frame for Medium Power SO20.

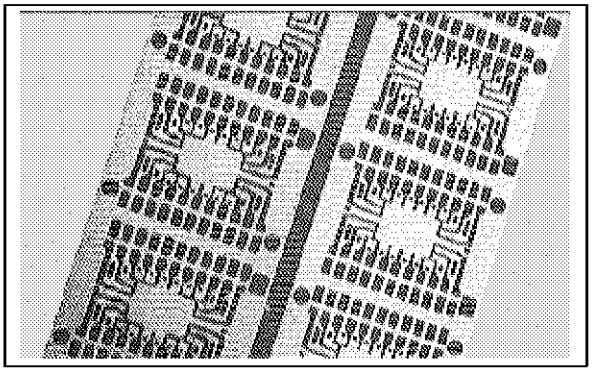


**Figure M1 :** Test Board for Medium Power PLCC44.

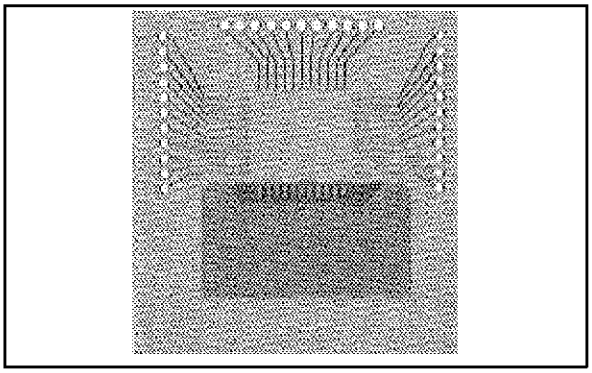
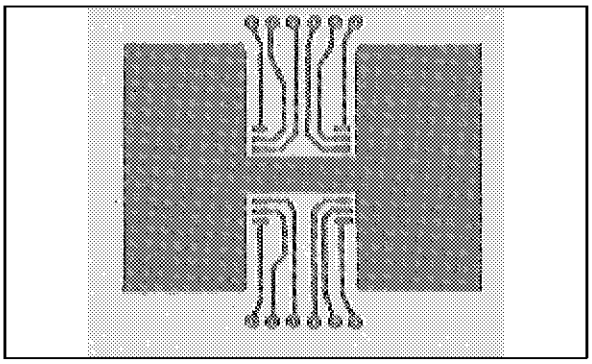


**Figure N1 :** Test Board for Medium Power SO20.



## THERMAL DATA OF SIGNAL PACKAGES

SUMMARY OF JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION (SGS-THOMSON test board)

| | +Die Size (millinches) | +Power PD [W] | +$R_{th(j-a)}$ [°C/W] on Board |
|---|---|---|---|
| SO8 Alloy 42<br>Copper | 90 x 100<br>94 x 125 | 0.2<br>0.2 | 250-310<br>130-180 |
| SO14 Alloy 42<br>Copper<br>Copper | 98 x 100<br>78 x 118<br>98 x 125 | 0.3<br>0.5<br>0.7 | 200-240<br>120-160<br>105-145 |
| SO16 Alloy 42<br>Copper | 98 x 118<br>94 x 185 | 0.3<br>0.5 | 180-215<br>95-135 |
| SO16W Copper | 120 x 160 | 0.7 | 90-112 |
| SO20 Copper | 140 x 220 | 0.7 | 77-97 |
| PLCC-20 Cu | 180 x 180 | 0.7 | 90-110 |
| PLCC-44 Cu | 260 x 260 | 1.5 | 50-60 |
| PLCC-68 Cu | 425 x 425 | 1.5 | 40-46 |
| PLCC-84 Cu | 450 x 450 | 2.0 | 36-41 |
| $R_{th(j-a)}$ values correspond to low and high board density | | | |

SUMMARY OF JUNCTION TO CASE THERMAL RESISTANCE

| | +Die Pad Size (millinches) | +$R_{th(j-a)}$ [°C/W] |
|---|---|---|
| PLCC20 | 140 x 140 | 25 |
| PLCC44 | 260 x 260 | 13 |
| PLCC68 | 425 x 425 | 10 |
| PLCC84 | 450 x 450 | 9 |

## JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION

**Figure 1 :** SO8.

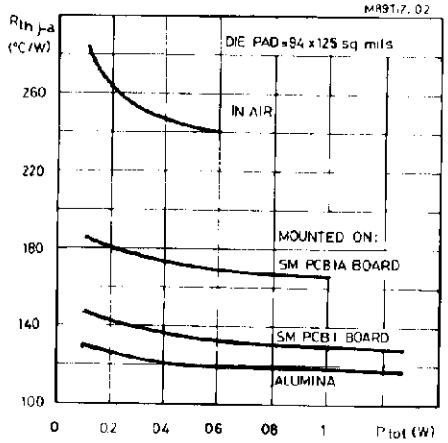



**Figure 2 :** SO14.

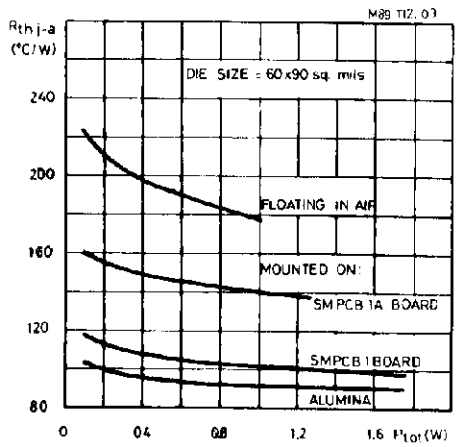


**Figure 3 :** SO16.

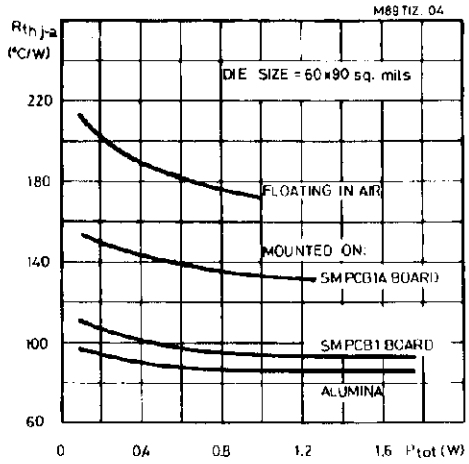



**Figure 4 :** SO20.

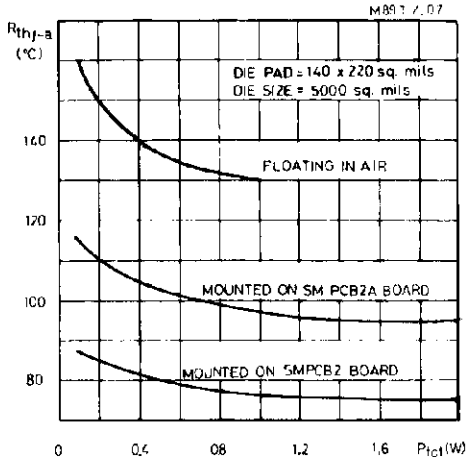



**Figure 5 :** PLCC20.

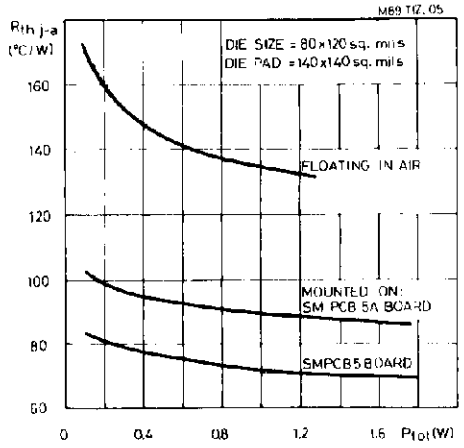



**Figure 6 :** PLCC44.

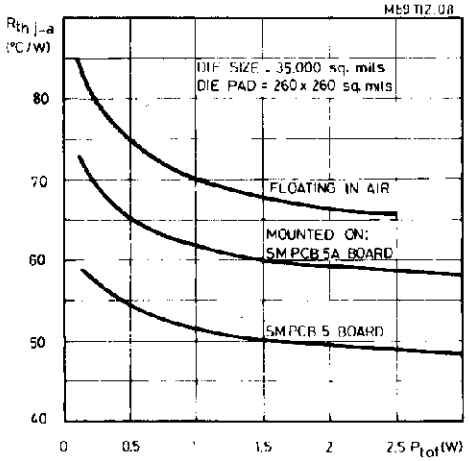



**Figure 7 :** PLCC68.

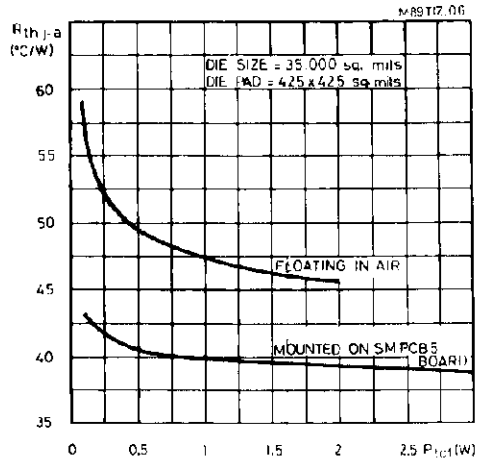
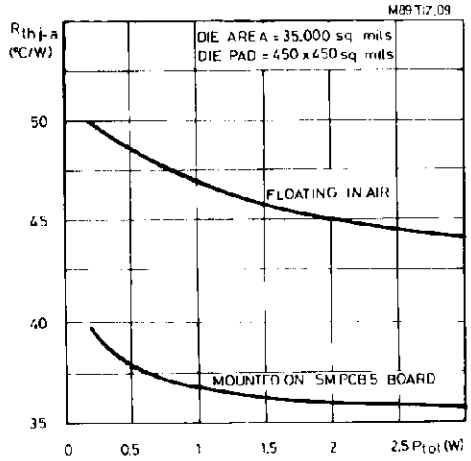



**Figure 8 :** PLCC84.



**JUNCTION TO AMBIENT THERMAL RESISTANCE VS BOARD LAY-OUT**
(area of copper tracks on the board)

**Figure 9 :** SO16.

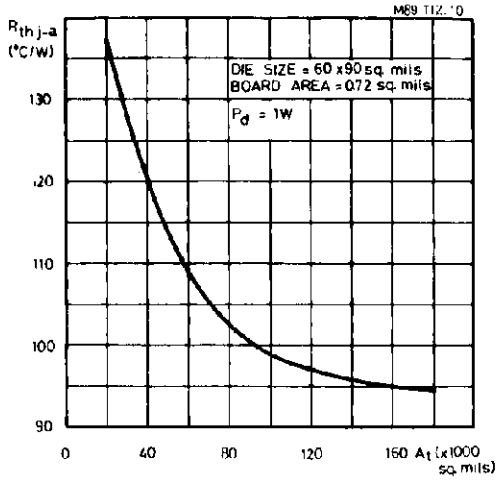



**Figure 10 :** SO20.

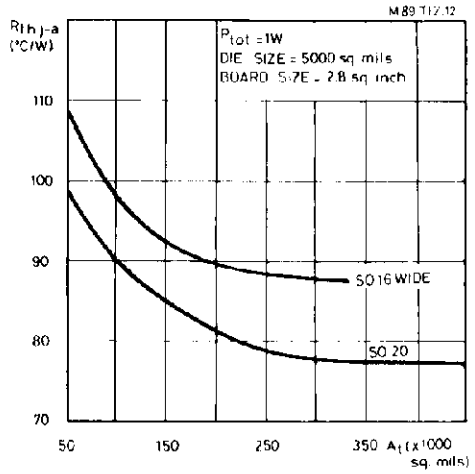



**Figure 11 :** PLCC44.

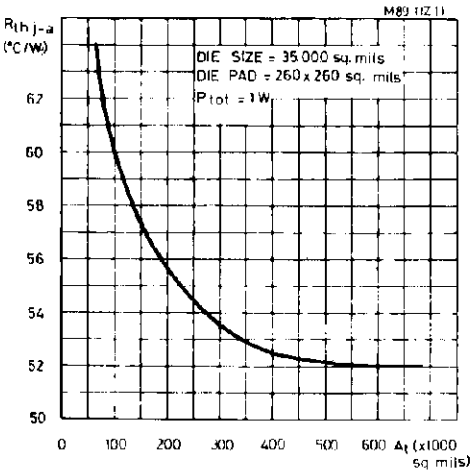
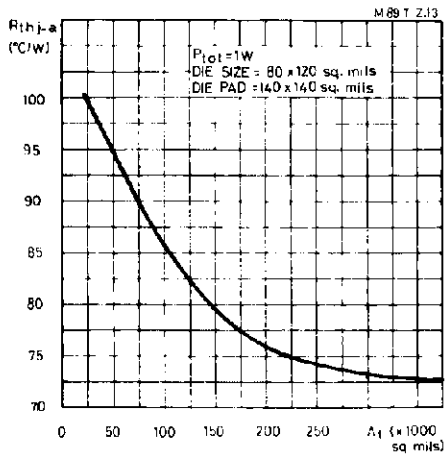



**Figure 12 :** PLCC20.



## TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

**Figure 13 :** SO8.

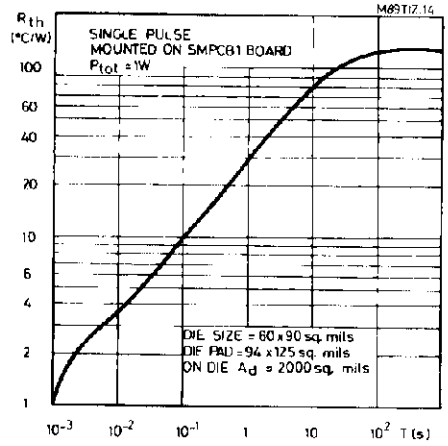



**Figure 14 :** SO14, 16.

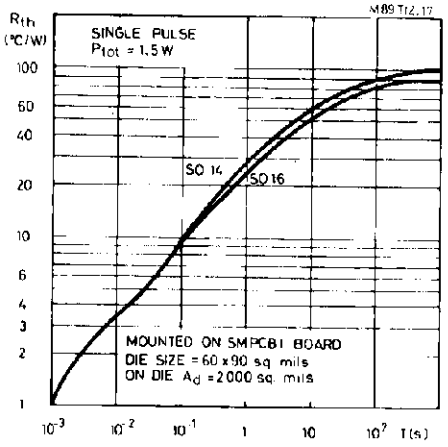



**Figure 15 :** SO20.

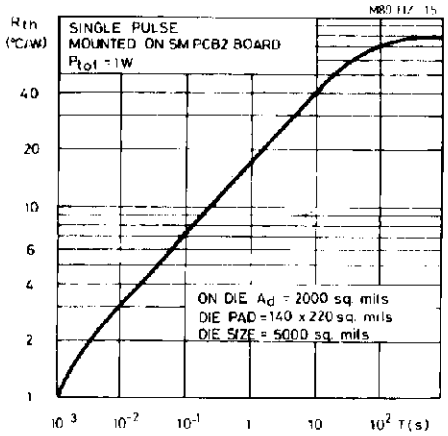



**Figure 16 :** PLCC44.

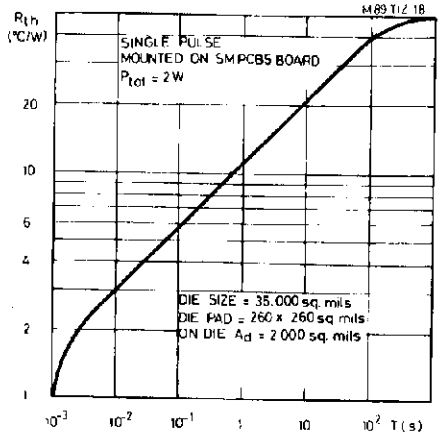



**Figure 17 :** PLCC68.

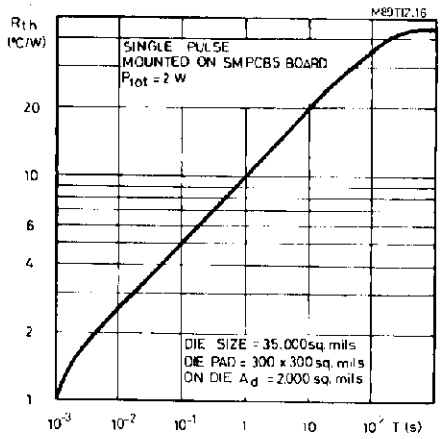
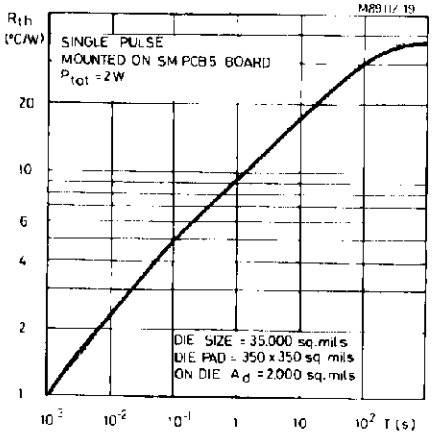



**Figure 18 :** PLCC84.



## PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

**Figure 19 :** SO14.

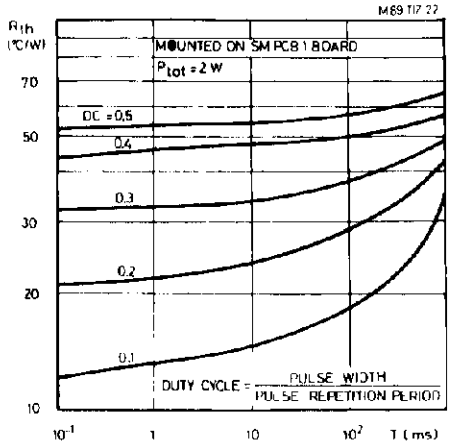



**Figure 20 :** SO20.

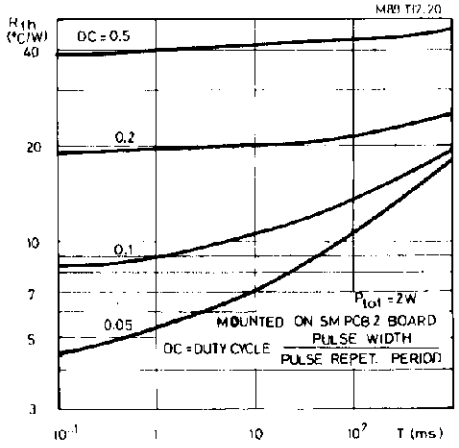



**Figure 21 :** PLCC44.

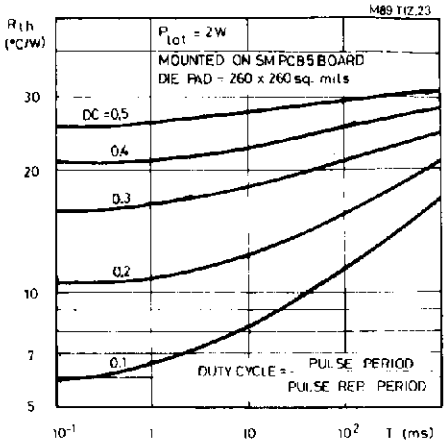



**Figure 22 :** PLCC68.

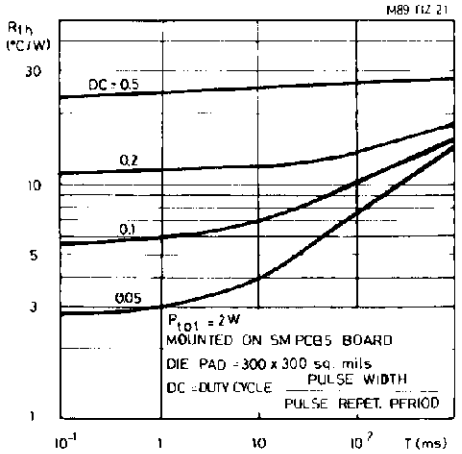
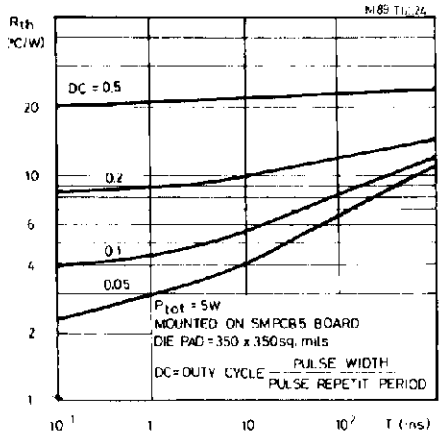



**Figure 23 :** PLCC84.



## THERMAL DATA OF MEDIUM POWER PACKAGES

| | $+R_{th(j-p)}$ [°C/W] (AVERAGE) | $+R_{th(j-a)*}$ [°C/W] |
|---|---|---|
| SO (12+4+4) | 14 | 50 |
| PLCC (33+11) | 12 | 41 |

* with 6 sq. cm. on board heat-sink.

## JUNCTION TO PINS THERMAL RESISTANCE VS ON DIE DISSIPATING AREA

**Figure 24 :** SO (12 + 4 + 4).

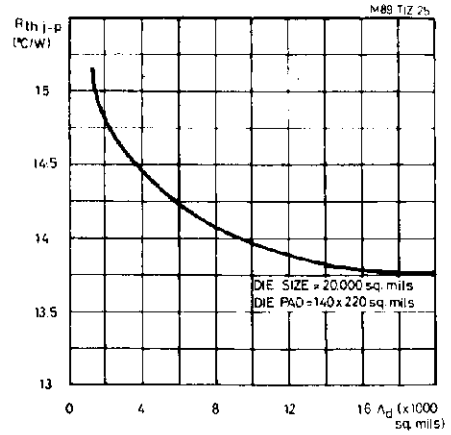
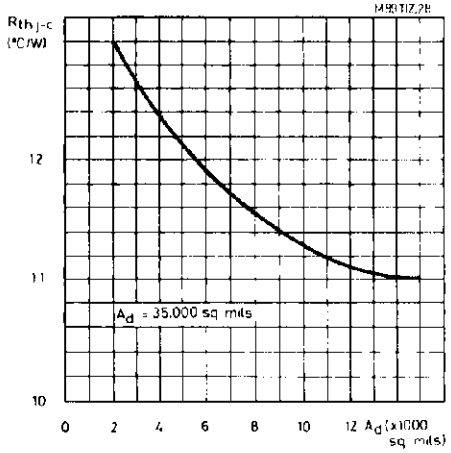
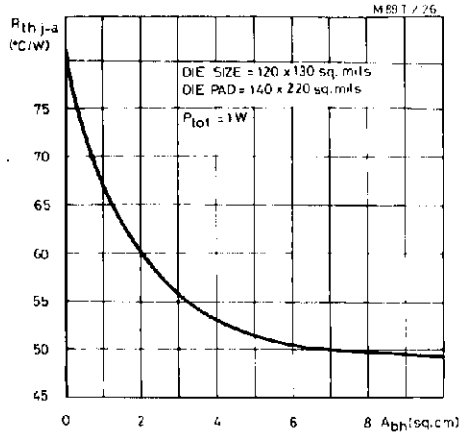



**Figure 25 :** PLCC (33 + 11).




## JUNCTION TO AMBIENT THERMAL RESISTANCE VS AREA ON BOARD HEAT-SINK

**Figure 26 :** SO (12 + 4 + 4).



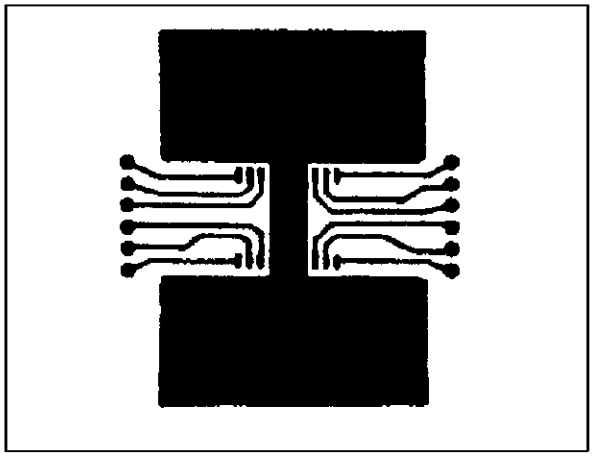
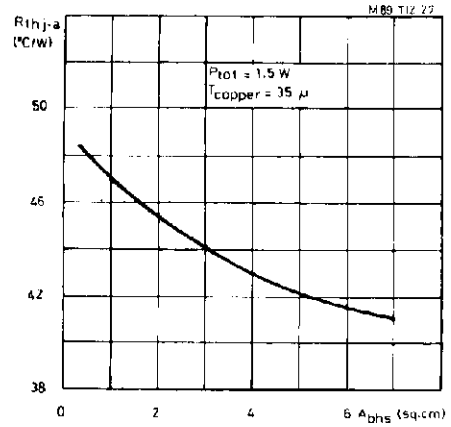
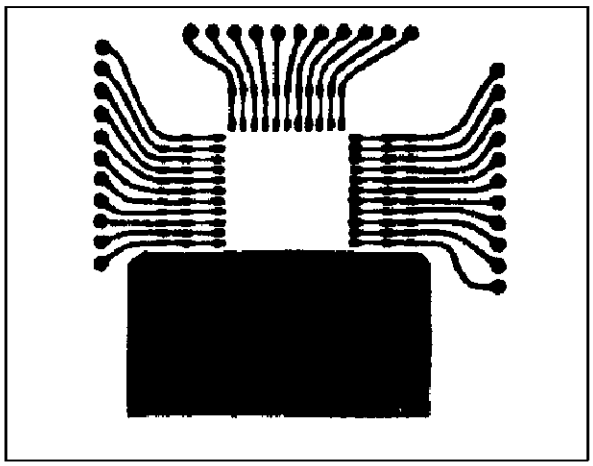



**Figure 27 :** PLCC (33 + 11).



## TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

**Figure 28 :** SO (12 + 4 + 4).

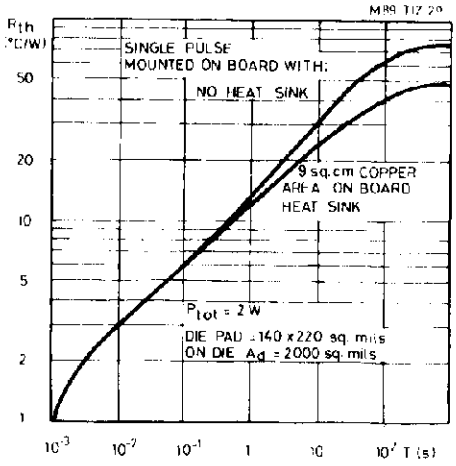
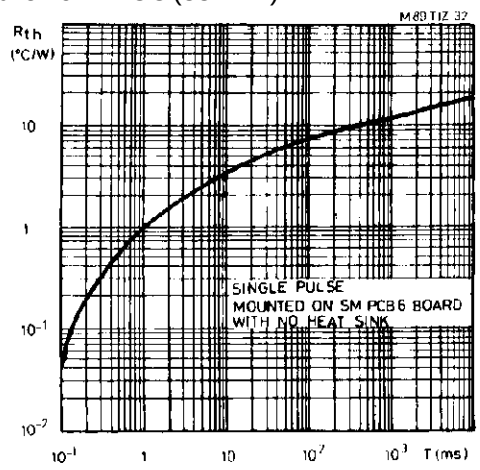
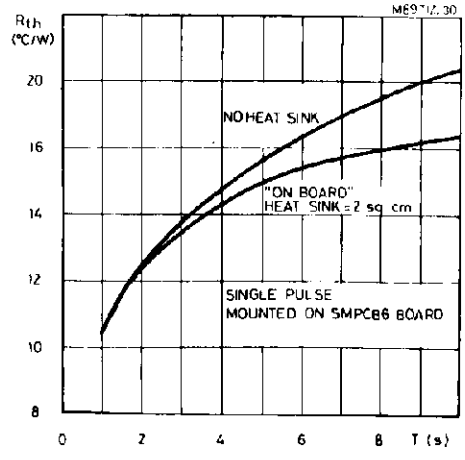



**Figure 29 :** PLCC (33 + 11).




pulse length = 0.1 – 10ms.

**Figure 30 :** PLCC (33 + 11).




pulse length = 1 – 10s.

## PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES.

**Figure 31 :** PLCC (12 + 4 + 4).

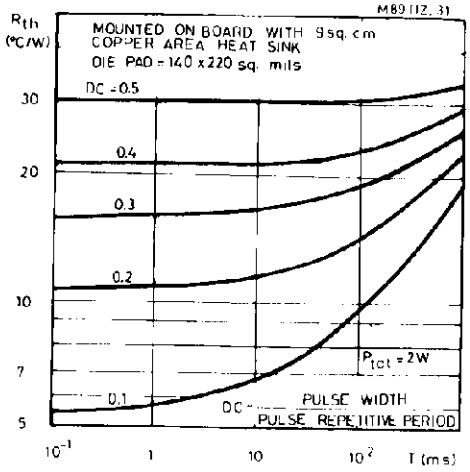
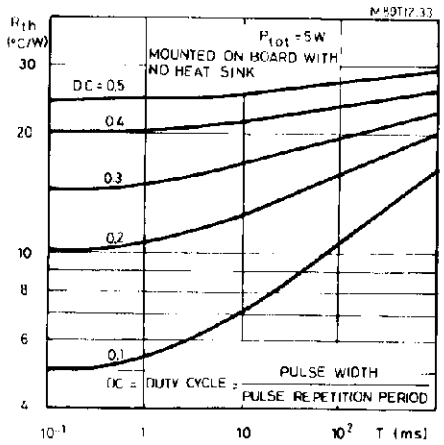



**Figure 32 :** PLCC (33 + 11).




## APPLICATION EXAMPLES OF THERMAL DATA

Good thermal design begins with system and reliability considerations. This turn is based on correct consideration of ambient and device temperature parameters.

The ambient temperature $T_a$ defined for applications can range from 50 to 55°C, as is common in many consumer and computer applications, through to 80°C or more in applications such as automotive systems. The ambient temperature depends on the various heat and cooling sources surrounding the device. An important factor in device lifetime is junction temperature - lifetime is approximately halved when junction temperature $T_j$ is increased by 10°C. The maximum junction temperature commensurate with good reliability, takes into account the activation energy of the failure mechanisms which may differ for various silicon and packaging technologies.

In plastic packages the maximum $T_{jmax}$ is 150°C, but lower values (100 to 120°C) may be specified in high rel applications such as telecoms.

When $T_{jmax}$ and $T_a$ are known, their difference $\Delta T_j$ indicates the permissible junction temeperature rise for a given device. For a given power dissipation Pd, the thermal design must ensure that the product Pd x Rth(j-a) is lower than $\Delta T_j$ ; where $R_{th(j-a)}$ is the thermal resistance of the device from the junction to the ambient at temperature $T_a$. This takes into consideration the many elements connected to the heat source and includes the leadframe, moulding compound, substrate and heatsink, if used.

**EXAMPLE 1 : Maximum dissipation for SO16 packaged device soldered onto an FR4 board (1 oz copper) under the following conditions :**

- Ambient temperature : $T_a$ = 70°C
- Maximum Junction Temperature : $T_{jmax}$ = 130°C

The average length of the 12mils wide copper line connected to each pin is 80mils, soldering pads are 30 x 40mils. The total are is thus :

A = [(80 x 12) + 1200 x 16] = 34560sq.mils

**SOLUTION**

From fig. 13, the value for $R_{th(j-a)}$ is 125°C/W for a copper frame package. Comparing figs. 5 and 6, a value of about 240°C/W can be assumed for Alloy 42 packages. The allowed rise in junction temperature is : $\Delta T_{jmax}$ = 130 - 70 = 60°C

Maximum dissipation is given by $\Delta Tjmax/R_{th(j-a)}$.

Therefore :

60/125 = 0.48W for Copper frame

60/240 = 0.25 for Alloy 42 frame

**EXAMPLE 2 : Junction temperature for an SO20 packaged device soldered on FR4, under the following conditions :**

- Ambient temperature $T_a$ = 70°C
- Dissipated Power Pd = 0.6W

**SOLUTION**

A total trace-area of 200k sq.mils is assumed,this then gives, from fig. 14 :

- Thermal Resistance $R_{th(j-a)}$ = 90°C/W
- $\Delta T_j = Pd \times R_{th(j-a)}$
- $\Delta T_j = 0.6 \times 90 = 54°C$
- Junction Temperature $T_j = 54 + 70 = 124°C$

**EXAMPLE 3 : To determine the size of an integrated heatsink for a medium power application using a PLCC (33 + 11) under the following conditions :**

- Ambient temperature $T_a$ = 50°C
- Max. Junction Temperature $T_{jmax}$ = 150°C
- Dissipated Power Pd = 2.2W

**SOLUTION**

By calculation the application needs an $R_{th(j-a)}$ of : (150 - 50)/2.2 = 45.5°C/W

From figure 32 the on board heatspreader can thus be defined as needing an area of about 2 sq.cm.

**EXAMPLE 4 : Given the application described in example 3 determine the maximum pulse width for a single 4W pulse superimposed on a continuous 1.5W dissipation**

**SOLUTION**

The continuous steady state junction temperature at 1.5W dissipation is :

$T_{jss}$ = (1.5 x 45.5) + 50 = 118.25°C

The single pulse is allowed to cause a maximum increase of (150 - 118.25°C) = 31.75°C.

The related transient thermal resistance is (31.75/4) = 7.9°C/W

From figure 33, the corresponding pulse width can be interpreted as being in the order of 200ms.

**EXAMPLE 5 : In a medium power application using an SO (12 + 4 + 4) calculate the average junction temperature and the peak temperature for repeated pulses under the following conditions :**

- Ambient temperature $T_a$ = 70°C
- On board heatsink area A = 9 sq.cm.
- Pulse length = 100ms
- Pulse height = 5W
- Duty cycle = 20%

**SOLUTION**

From figure 31, the thermal resistance is found to be 49°C/W. Thus the average junction temperature can be calculated :

$T_{javg}$ = (5 x 49 x 0.2) + 70 = 119°C

From figure 36, the peak thermal resistance is given as around 15°C/W. The peak temperature can thus be calculated as :

$T_p$ = (5 x 15) + 70 = 145